LCD Module User Manual

Customer	:	
MASS PRODUCTION CODE	:	**TC1602J-01WD0**
DRAWING NO.	:	**m-TC1602J-01WD0_A00**

Approved By Customer:

Date:

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1. Precautions in Use of LCD Module

(1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
(2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD Module.
(3) Don't disassemble the LCM.
(4) Don't operate it above the absolute maximum rating.
(5) Don't drop, bend or twist LCM.
(6) Soldering: only to the I/O terminals.
(7) Storage: please storage in anti-static electricity container and clean environment.

2. General Specification

ITEM	STANDARD VALUE	UNIT
Number of dots	16X2 CHARs	Dots
Outline dimension	84.0(W)X44.0(H)X12.8MAX.(T)	mm
View area	65.0(W)X16.0(H)	mm
Active area	56.21(W)X11.5(H)	mm
Dot size	0.56(W)X0.66(H)	mm
Dot pitch	0.60(W)X0.70(H)	mm
LCD type	STN, Yellow-green,positive,Transflective	
View direction	6 o'clock	
Backlight	LED, White	
MPU interface	4-SPI(Default status) Option:Parallel or 3-SPI	
DC-DC invertor	None	

3. Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T_{OP}	-20	-	+30	℃
Storage Temperature	T_{ST}	-30	-	+80	℃
Input Voltage	V_I	0	-	V_{DD}	V
Supply Voltage For Logic	V_{DD}	0	-	5.5	V
Supply Voltage For LCD	V_{DD}-V_{EE}	0	-	5	V

4. Electrical Characteristics

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Voltage	V_{DD}-V_{SS}	-	4.7	5.0	5.2	V
Supply Volt.For LCD	V_{DD}-V_O	Ta=25℃	---	4.5	---	V
Input High Volt.	V_{IH}	-	2.0	-	V_{DD}	V
Input Low Volt.	V_{IL}	-	-0.3	-	0.8	V
Output High Volt.	V_{OH}	I_{oH}=-0.2mA	2.4	-	V_{DD}	V
Output Low Volt.	V_{OL}	I_{oL}=1.6mA	0	-	0.4	V
Supply Current	I_{DD}	-	---	1.0	---	mA

5. Backlight Information

Absolute Maximum ratings (Ta=25℃)

Item	Symbol	Conditions	Rating	Unit
Reverse voltage	Vr	-	5.0	V
Reverse Current	I_r	Vr=5.0V	80	uA
Absolute maximum forward Current	Ifm		100	mA
Peak forward current	Ifp	I msec plus 10% Duty Cycle	240	mA
Power dissipation	P_d		340	mW
Operating Temperature Range	T_{oper}		-30~+70	℃
Storage Temperature Range	Tst		-40~+80	℃

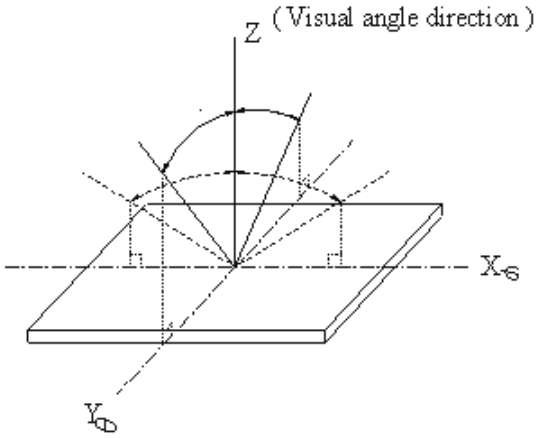
Electrical/Optical Characteristics (Ta=25^{0}C,If=40mA)

Color	Wavelength λp(nm)	Spectral line half width Δλ (nm)	Operating Voltage(V) (±0.15V)	Forward Current (mA)
White	---	---	3.1	30

6. Optical Characteristics

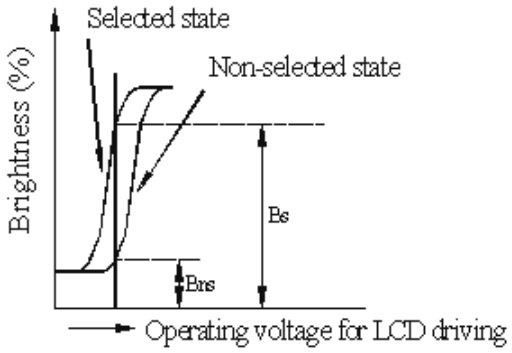
ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
View Angle	(V) θ	CR≧2	10	–	120	deg.
	(H) ϕ	CR≧2	-45	–	45	deg.
Contrast Ratio	CR	–	–	5	–	–
Response Time	T rise	–	–	200	300	ms
	T fall	–	–	150	200	ms

■View Angles

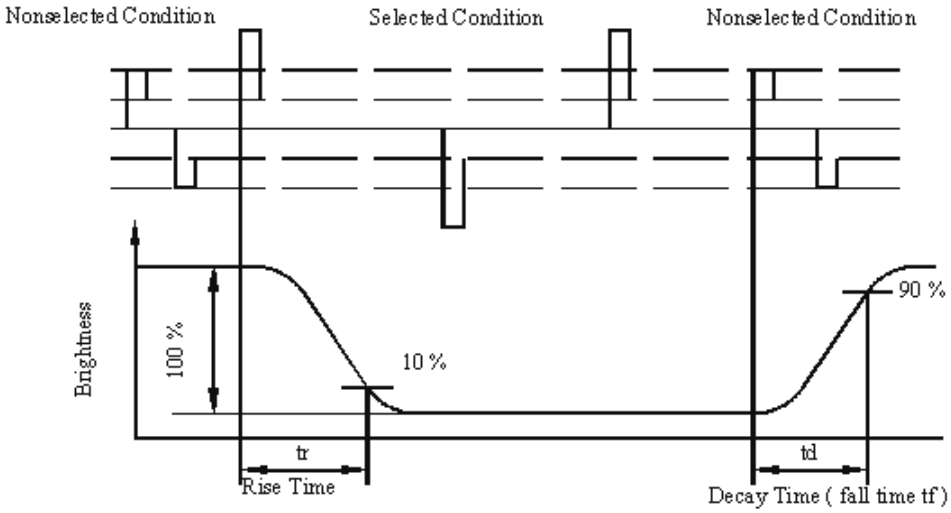


■Contrast Ratio

$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



■Response time



7.Interface Description

Parallel mode(Jps shorted to "P")

Pin No.	Symbol	Level	Description
1	V_{SS}	0V	Ground
2	V_{DD}	+5.0V	Power supply for Logic
3	V_O	(Variable)	Driving voltage for LCD
4	RS(D/I,A0)	H/L	H:Data L :Instruction
5	RW	H/L	H:Read L:Write
6	E	H/L	Enable signal
7~14	DB0~DB7	H/L	Data bus. DB7 is used for Busy Flag .
15	A(LED+)	+5.0V	Anode of LED Backlight
16	K(LED-)	0V	Cathode of LED Backlight
17	/RST	L	Active low
18	PSB	H	Interface type selection,H: Parallel interface

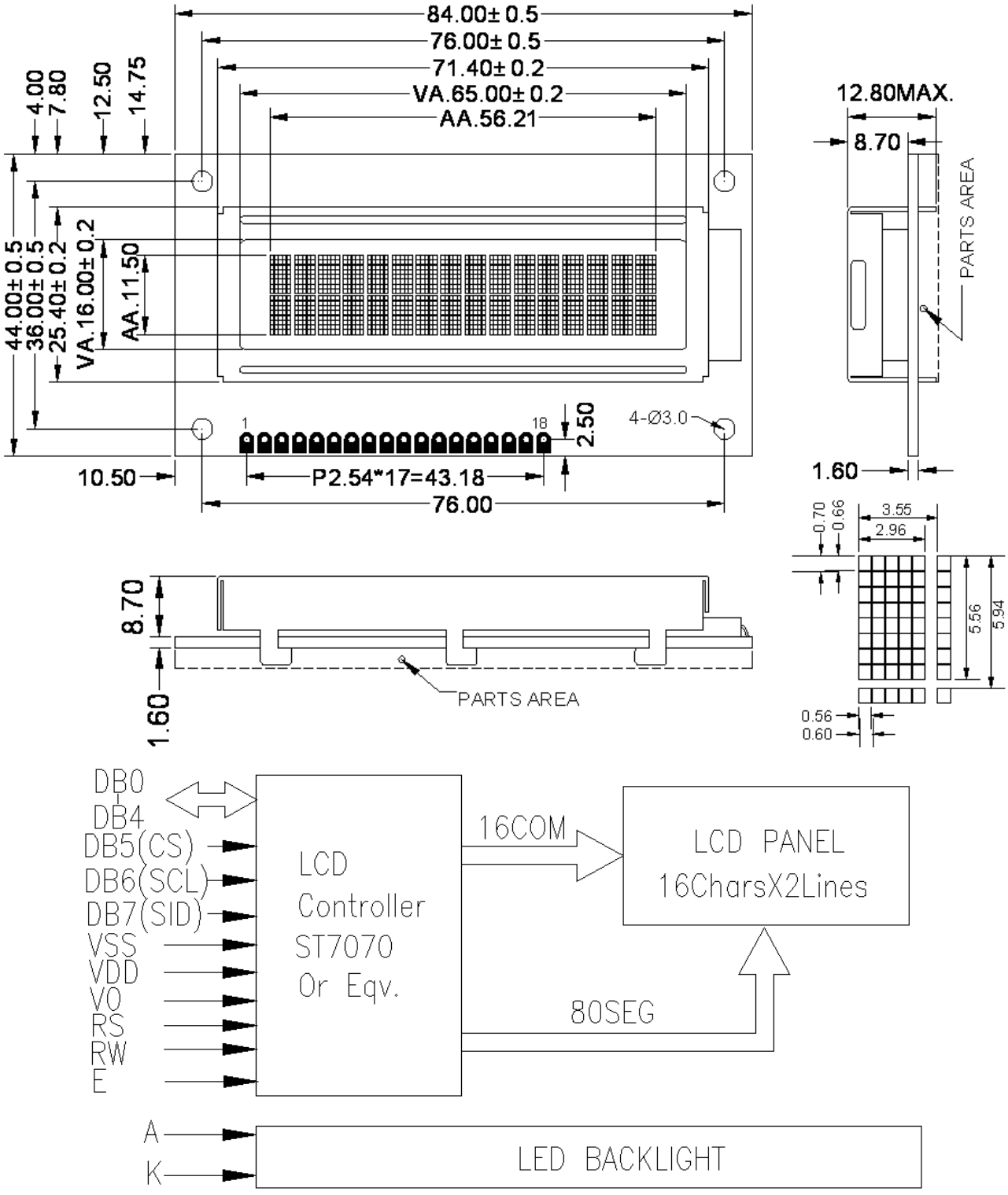
4-SPI mode(Jps shorted to "S",Default status)

Pin No.	Symbol	Level	Description
1	V_{SS}	0V	Ground
2	V_{DD}	+5.0V	Power supply for Logic
3	V_O	(Variable)	Driving voltage for LCD
4	RS(D/I,A0)	H/L	H:Data L :Instruction
5	V_{SS}	0V	Ground
6~11	VDD	+5.0V	VDD
12	CS(DB5)	L	Chip select, active low
13	SCL(DB6)	H/L	Serial clock input
14	SID(DB7)	H/L	Serial data input
15	A(LED+)	+5V	Anode of LED Backlight
16	K(LED-)	0V	Cathode of LED Backlight
17	/RST	L	Active low
18	PSB	L	Interface type selection,L: Serial interface

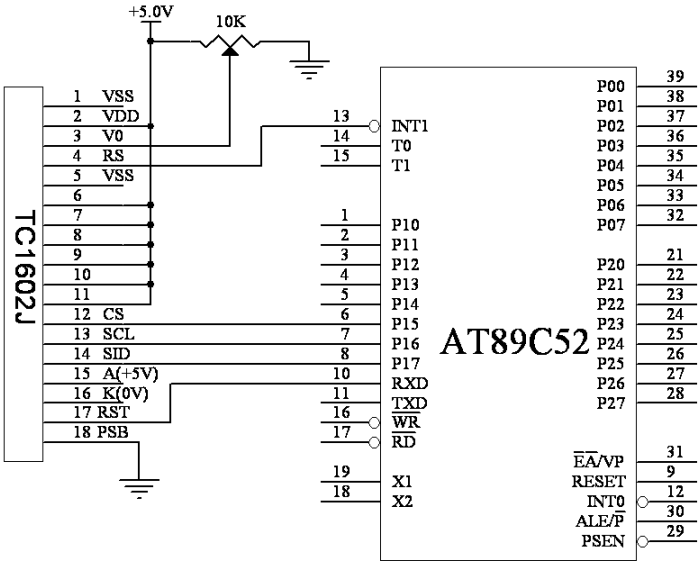
3-SPI mode(Jps shorted to "S",Default status)

Pin No.	Symbol	Level	Description
1	V_{SS}	0V	Ground
2	V_{DD}	+5.0V	Power supply for Logic
3	V_O	(Variable)	Driving voltage for LCD
4~5	V_{SS}	0V	Ground
6~11	VDD	+5.0V	VDD
12	CS(DB5)	L	Chip select, active low
13	SCL(DB6)	H/L	Serial clock input
14	SID(DB7)	H/L	Serial data input
15	A(LED+)	+5.0V	Anode of LED Backlight
16	K(LED-)	0V	Cathode of LED Backlight
17	/RST	L	Active low
18	PSB	L	Interface type selection,L: Serial interface

8. Contour Drawing & Block Diagram



9.Application circuit



10. LCM Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

Various Kinds of Operations according to RS and R/W Bits

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB6 to DB0)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

When the **BF= "High"**, it indicates that the LCM internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is **not High**.

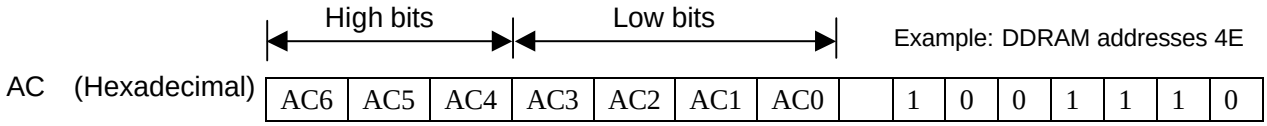
Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 - DB6 ports.

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80x8 bits,or 80 charcters.Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



LCM DDRAM Address(In HEX)

16 Chars X 2 Lines Display															
No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd Line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See “Standard Character pattern”.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM) shown below

Char Code(DDRAM data)								CGRAM address						CGRAM data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	X	X	X	0	1	1	1	0	Pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
0	0	0	0	X	1	1	1	1	1	1	0	0	0	X	X	X	1	0	0	0	1	Pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

“ X”: don’t care

11. User instruction Definitions

11.1 Instruction table

This LCM can select basic or extended instruction set by “Function set” Instruction,see detail in “Function set” description.When EXT=0,only basic instruction can be executed, When EXT=0,only basic instruction can be executed,
When EXT=1,only extended instruction can be executed,

Instruction	Instruction Code										Description	Execution time f_{osc}=270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
EXT=0 or EXT=1(Can be executed both in basic or extended instruction mode)												
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM and set DDRAM address to “00H” from AC.	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	0μ s
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	37μ s
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37μ s
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length(DL:4-bit/8-bit), numbers of display line(N: 1-line/2-line), display font type(F: 5X8 dots/ 5X11 dots)	37μ s
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or can not be known by reading BF. The contents of address counter can also be read.	0μ s
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM DDRAM/CGRAM).	37μ s
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	37μ s
EXT=0 (Can be executed in basic instruction mode only)												
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37μ s
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	37μ s
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	37μ s

Remark: ‘ X ’ don’t care

Instruction	Instruction Code										Description	Execution time f_{OSC}=270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
EXT=1 (Can be executed in extended instruction mode only)												
Bias resistor select	0	0	0	0	0	0	0	1	Rb1	Rb0	Used internal resister only provide 1/5 bias mode Rb[1:0]=00-> External Resister. Rb[1:0]=01~11->Internal Resister	37μ s
COM,SEG direction select	0	0	0	0	0	0	C1	C2	S1	S2	C1:COM1~8-> COM8~1 C2:COM9~16-> COM16~9 S1:SEG1~40->SEG40~1 C2:SEG41~80->SEG80~41	37μ s
Set display data length	0	0	1	L6	L5	L4	L3	L2	L1	L0	To specify the number ofdata bytes(3-wire SPI mode)	37μ s

Note:

In the parallel Interface,be sure the LCM is not in the busy state (BF = 0) before sending an instruction from the MPU to the LCM. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

11.2 Instruction Description

EXT=0 or EXT=1(Can be executed in basic or extended instruction mode)

1)Clear Display

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status. Namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

2) Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

3) Display ON/OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display / cursor / blink ON / OFF 1 bit register.

D: Display ON / OFF control bit

When D = "High", entire display is turned on.

When D = "Low", display is turned off, but display data is remained in DDRAM.

C: Cursor ON / OFF control bit

When C = "High", cursor is turned on.

When C = "Low", Cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON / OFF control bit

When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.

When B = "Low", blink is off.

4) Cursor or Display Shift

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display Without Writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. (refer to Table 4) During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Operation
0	0	Shift the cursor to the left, AC is decreased by 1.
0	1	Shift the cursor to the right, AC is increased by 1.
1	0	Shift all the display to the left, cursor moves according to the display.
1	1	Shift all the display to the right, cursor moves according to the display.

5) Function Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	EXT	-	-

DL: Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

EXT: Select basic or extended instruction set

When EXT="L" the commands 'Entry Mode Set','Set CGRAM address' and 'Set DDRAM address' can be performed ,

when EXT="H" the commands 'Bias resistor select', 'COM、SEG direction select' and 'Set display data length' can be performed.

Other command can be executed in both cases.

6) Read Busy Flag & Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether LCM is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

7) Write data to RAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

8) Read data from DDRAM or CGRAM

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

EXT=0 (Can be executed in basic instruction mode only)

9)Entry Mode Set

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment / decrement of DDRAM address (cursor or blink)

When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.

* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

SH: Shift of entire display

When DDRAM read (CGRAM read / write) operation or SH = "Low", shift of entire display is not performed. If SH = "High" and DDRAM write operation, shift of entire display is performed according to I/D value:

I/D ="1" : shift left,

I/D = "0" : shift right.

10) Set CGRAM Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

11) Set DDRAM Address

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1), DDRAM address is the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

EXT=1 (Can be executed in extended instruction mode only)

12) Bias resistor select

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	Rb1	Rb0

This LCM controller built-in internal bias resistor,set by follow table

Rb1	Rb0	Description
0	0	External bias resistor select.
0	1	Build-in resistor select (R=2.2K).
1	0	Build-in resistor select (R=6.8K).
1	1	Build-in resistor select (R=9.0K).

13) COM,SEG direction select

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	C1	C2	S1	S2

The SEG and COM output in this LCM all have bi-direction control by the register.

COM output:

COM output C1	COM1----------COM8
0	COM1->Common address->COM8
1	COM8->Common address->COM1

COM output C2	COM9----------COM16
0	COM19->Common address->COM16
1	COM16->Common address->COM9

SEG output:

SEG output S1	SEG1----------SEG40
0	SEG1-> Segment Address->SEG40
1	SEG40-> Segment Address->SEG1

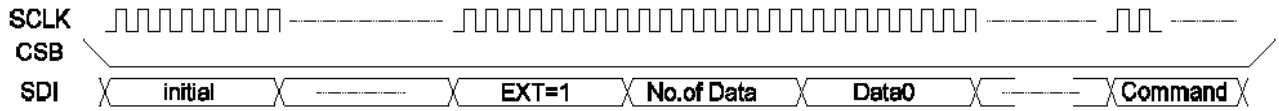
SEG output S2	SEG41----------SEG80
0	SEG41-> Segment Address->SEG80
1	SEG80-> Segment Address->SEG41

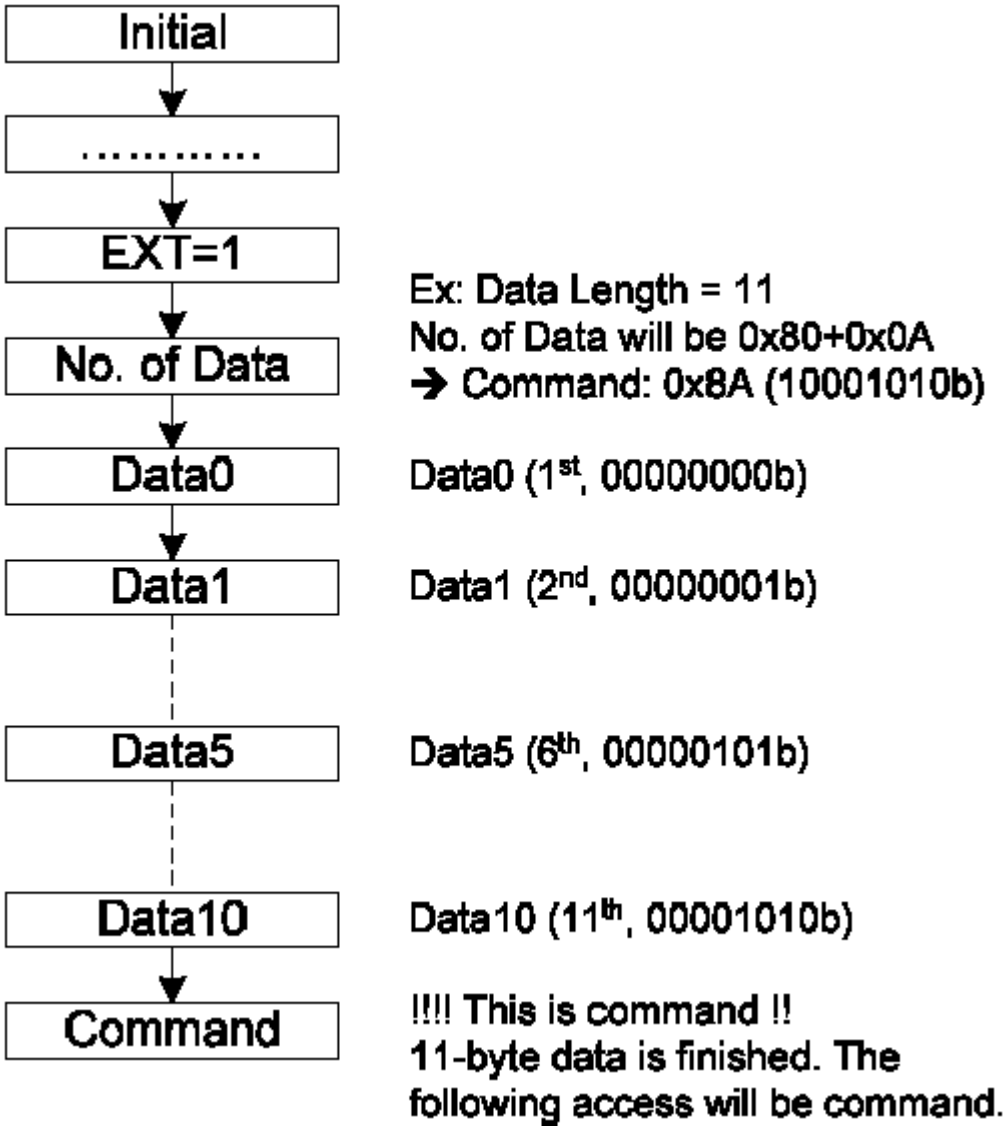
14) Set display data length(Only in 3line-SPI interface)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	L6	L5	L4	L3	L2	L1	L0

L6	L5	L4	L3	L2	L1	L0	**Data length**
0	0	0	0	0	0	0	**1**
0	0	0	0	0	0	1	**2**
…	…	…	…	…	…	…	**…**
1	0	0	1	1	1	0	**79**
1	0	0	1	1	1	1	**80**

Only in 3line-SPI interface will use the register to set the number of display data(Max=4F). To write data to DDRAM , send Data Direction Command in 3-pin SPI . Data is latched at the rising edge of SCLK . And the DDRAM column address pointer will be increased by one automatically.





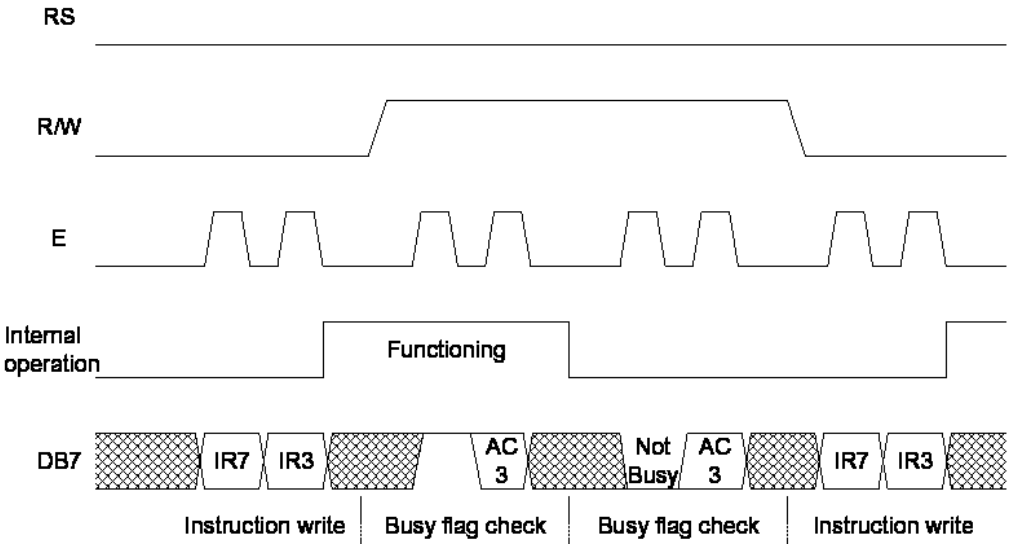
12.Interfacing to the MPU

The LCM can send data in either two 4-bit operations or one 8-bit operation or serial operation, thus allowing interfacing with 4- or 8-bit or serial MPU.

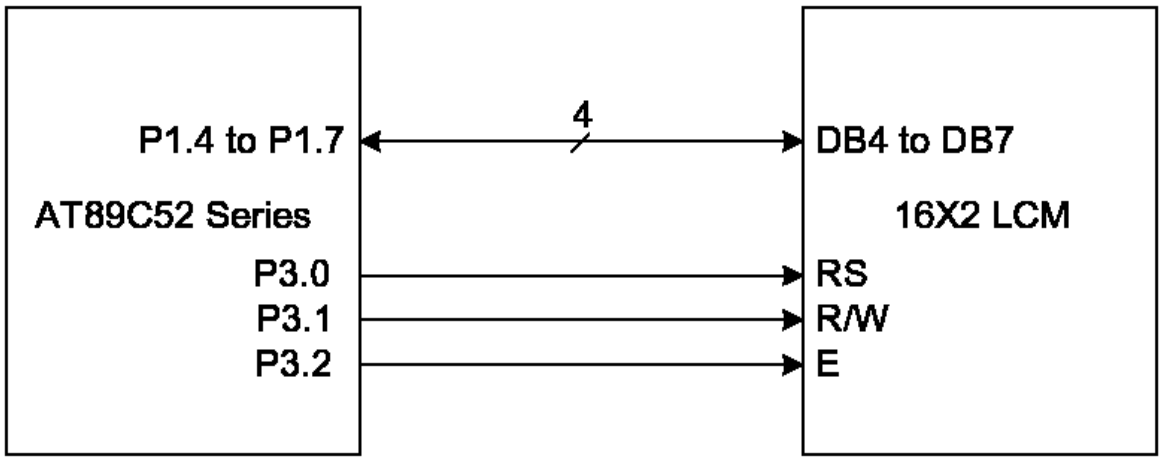
- **For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer.**

Bus lines DB0 to DB3 are disabled. The data transfer between the ST7070 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

Example of busy flag check timing sequence

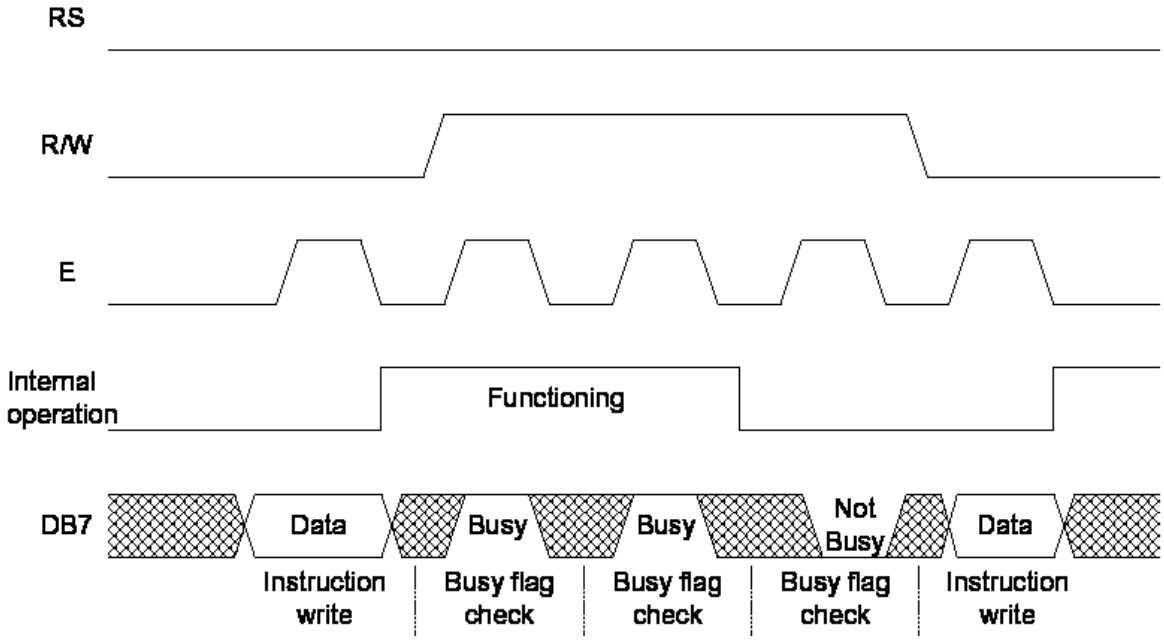


Intel 8051 interface

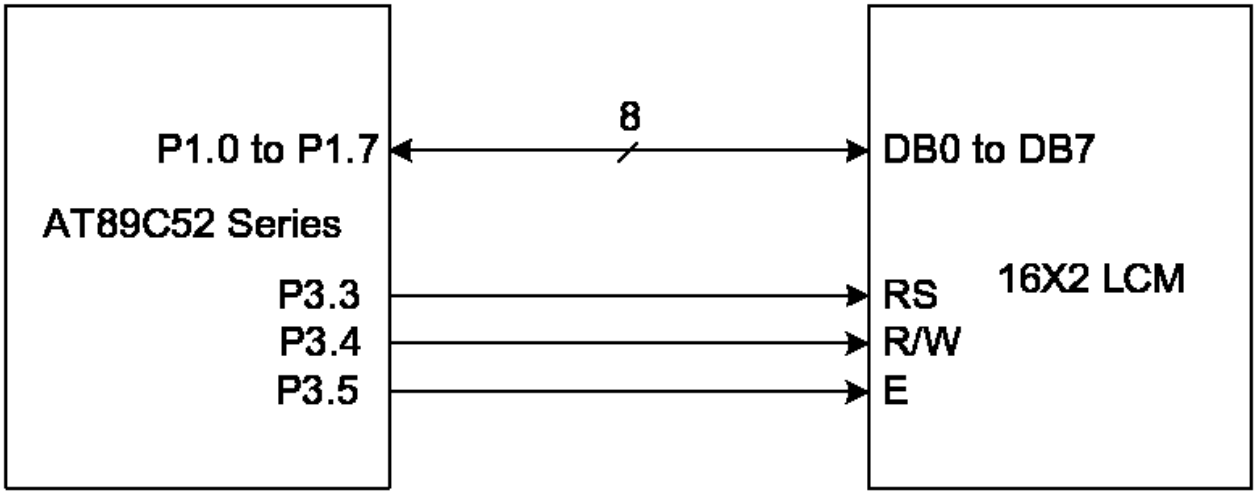


- **For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.**

Example of Busy Flag check timing sequence

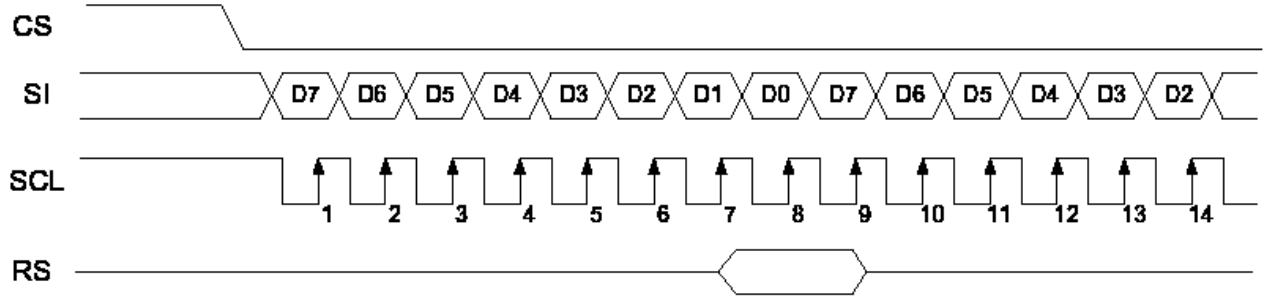


Intel 8051 interface

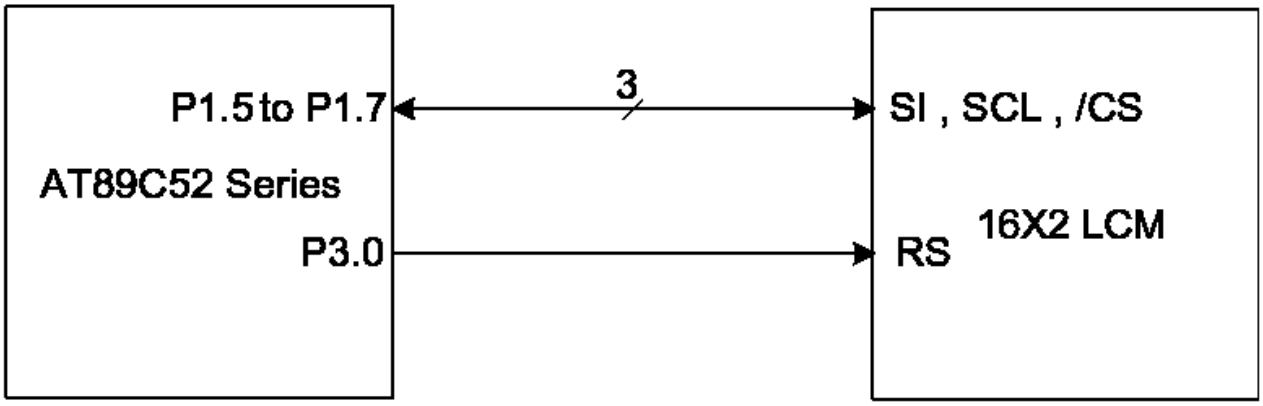


- **For serial interface data, bus lines (DB5 to DB7) are used. 4-Pin SPI**

Example of timing sequence

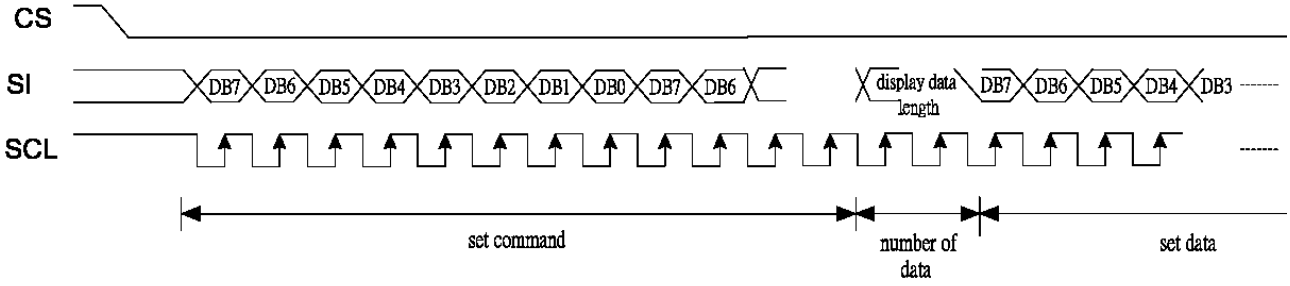


Intel 8051 interface

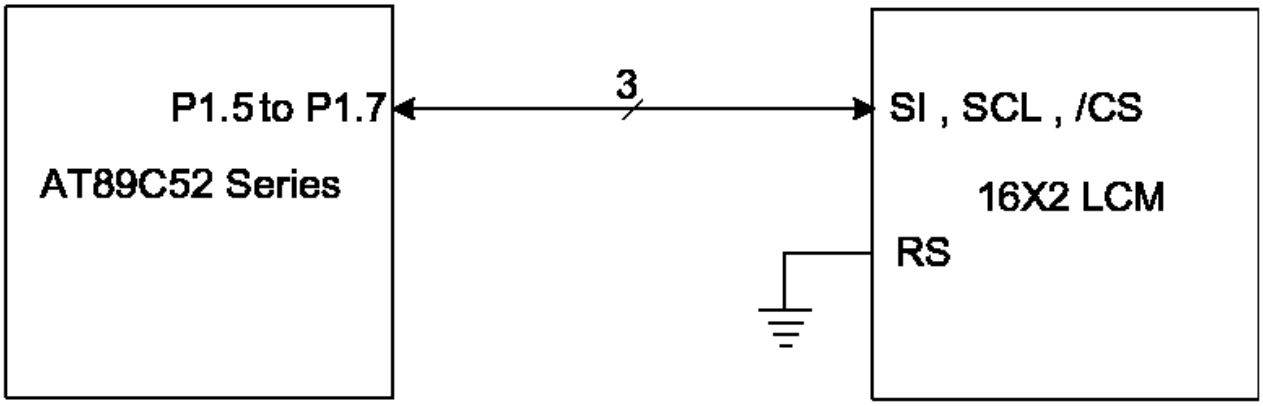


- **For serial interface data, bus lines (DB5 to DB7) are used. 3-Pin SPI**

Example of timing sequence

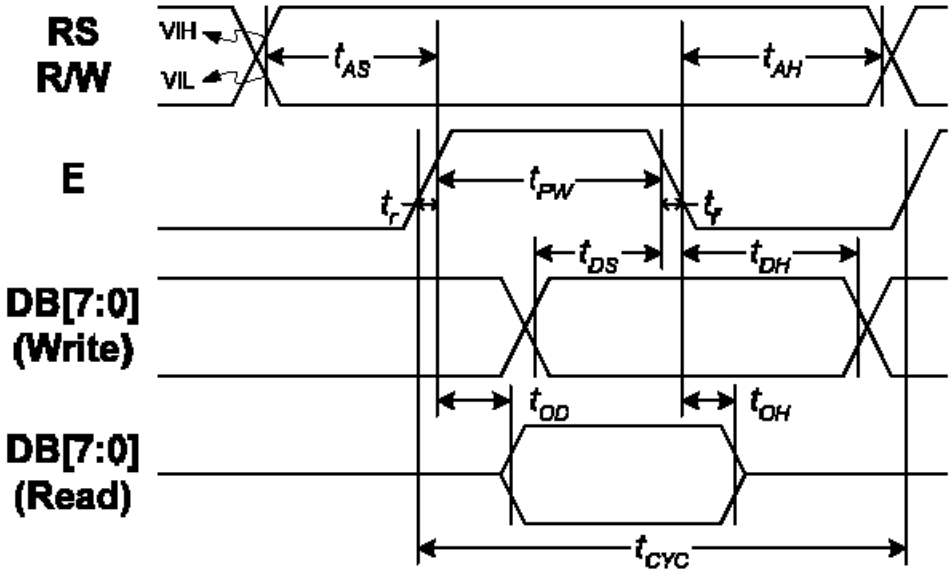


Intel 8051 interface

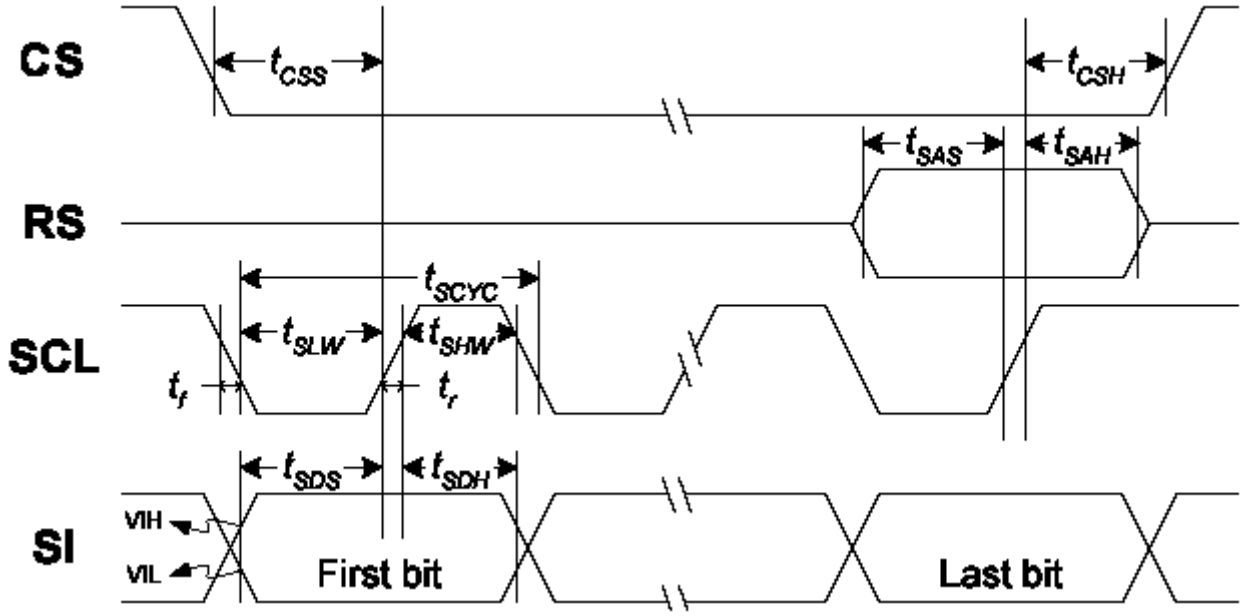


13. Timing Characteristics

- **Parallel Interface Write/Read by MPU**



- **Writing data from MPU to LCM (Serial)**



Parallel interface (TA = 25℃, VCC = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 75KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
Tr,Tf	Rise/Fall Time	-	-	-	0.2	µs
Write Mode (Writing data from MPU to LCM)						
T_{CYC}	Enable Cycle Time	Pin E (except clear display)	60	-	-	us
T_{PW}	Enable Pulse Width	Pin E	30	-	-	ns
Tr,Tf	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW	10	-	-	ns
T_{DS}	Data Setup Time	Pins: DB0 - DB7	30	-	-	ns
T_{DH}	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from LCM to MPU)						
T_{CYC}	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	480	-	-	ns
Tr,Tf	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW	10	-	-	ns
T_{OD}	Output Delay Time	Pins: DB0 - DB7	-	-	420	ns
T_{OH}	Output Hold Time	Pins: DB0 - DB7	10	-	-	ns

Parallel interface (TA = 25℃, VCC = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 91KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
Tr,Tf	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to LCM)						
T_{CYC}	Enable Cycle Time	Pin E (except clear display)	40	-	-	us
T_{PW}	Enable Pulse Width	Pin E	20	-	-	ns
Tr,Tf	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DS}	Data Setup Time	Pins: DB0 - DB7	20	-	-	ns
T_{DH}	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from LCM to MPU)						
T_{CYC}	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	430	-	-	ns
Tr,Tf	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{OD}	Output Delay Time	Pins: DB0 - DB7	-	-	390	ns
T_{OH}	Output Hold Time	Pins: DB0 - DB7	10	-	-	ns

Serial interface (TA = 25℃, VCC = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 75KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
Tr,Tf	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to LCM)						
T_{SCYC}	SCL Cycle Time	SCL	2480	-	-	ns
$T_{SHW,SLW}$	SCL Pulse Width	SCL	1190	-	-	ns
Tr,Tf	SCL Rise/Fall Time	SCL	-	-	25	ns
T_{SAS}	Address Setup Time	RS	75	-	-	ns
T_{SAH}	Address Hold Time	RS	10	-	-	ns
T_{SDS}	Data Setup Time	SI	10	-	-	ns
T_{SDH}	Data Hold Time	SI	75	-	-	ns
T_{CSS}	CS-SCL Time	CS	75			ns
T_{CSH}	CS-SCL Time	CS	250			ns

Serial Interface (TA = 25℃, VCC = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 91KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
Tr,Tf	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to ST7070)						
T_{SCYC}	SCL Cycle Time	SCL	2010	-	-	ns
$T_{SHW,SLW}$	SCL Pulse Width	SCL	1010	-	-	ns
Tr,Tf	SCL Rise/Fall Time	SCL	-	-	25	ns
T_{SAS}	Address Setup Time	RS	60	-	-	ns
T_{SAH}	Address Hold Time	RS	10	-	-	ns
T_{SDS}	Data Setup Time	SI	10	-	-	ns
T_{SDH}	Data Hold Time	SI	60	-	-	ns
T_{CSS}	CS-SCL Time	CS	60			ns
T_{CSH}	CS-SCL Time	CS	160			ns

14. Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the LCM when the power is turned on or hardware reset pin has low. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 40 ms after VCC rises to 4.5 V.

1.Display clear

2.Function set:

DL = 1; 8-bit interface data

N = 1; 2-line display

EXT=0;disable extension instruction.

3. Display on/off control:

D = 0; Display off

C = 0; Cursor off

P = 0; Page 1 of font table(DDRAM data b8=0)

4. Entry mode set:

I/D = 1; Increment by 1

S = 0; No shift

5. Bias resistor select:

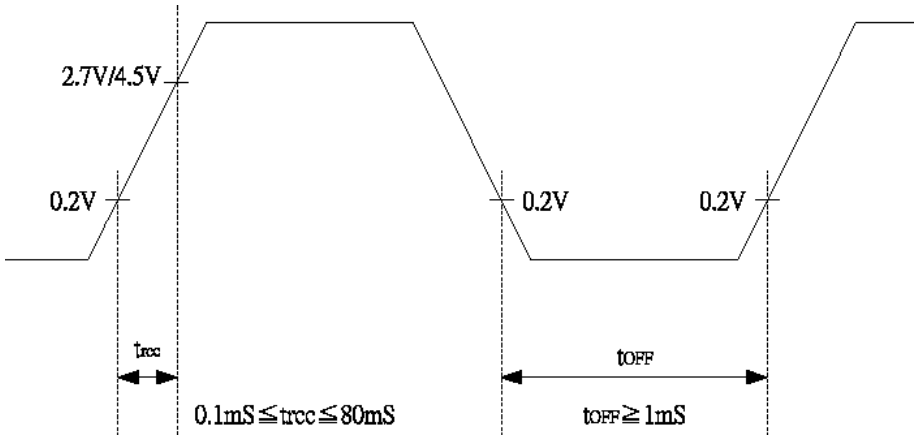
Rb1=0;Rb2=0 select external bias resistor.

6. COM、SEG direction select:

C1=0;C2=0;S1=0;S2=0 not reverse.

Note:

If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the LCM. For such a case, initialization must be performed by the MPU as explain by the following figure.

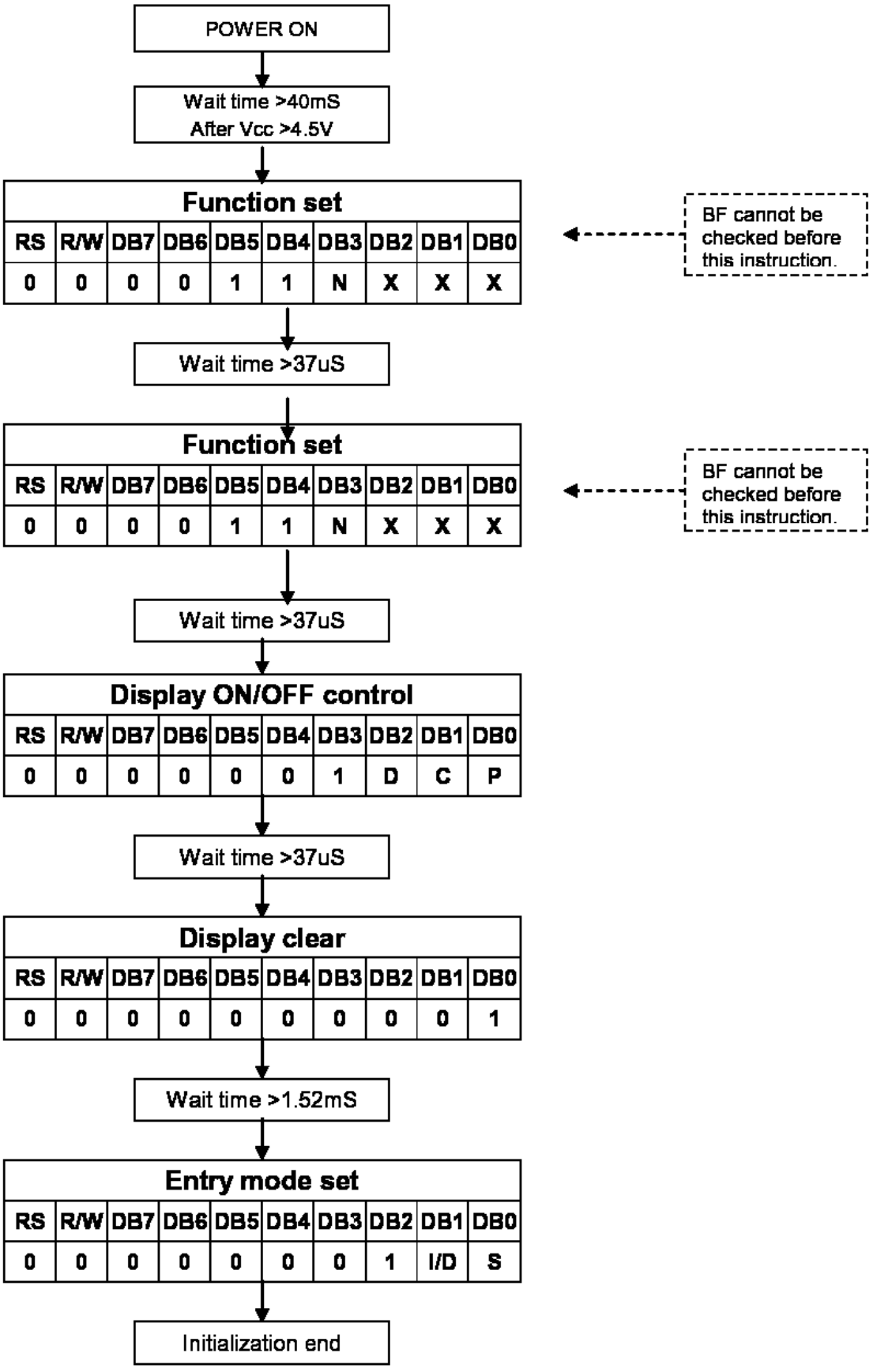


Note:

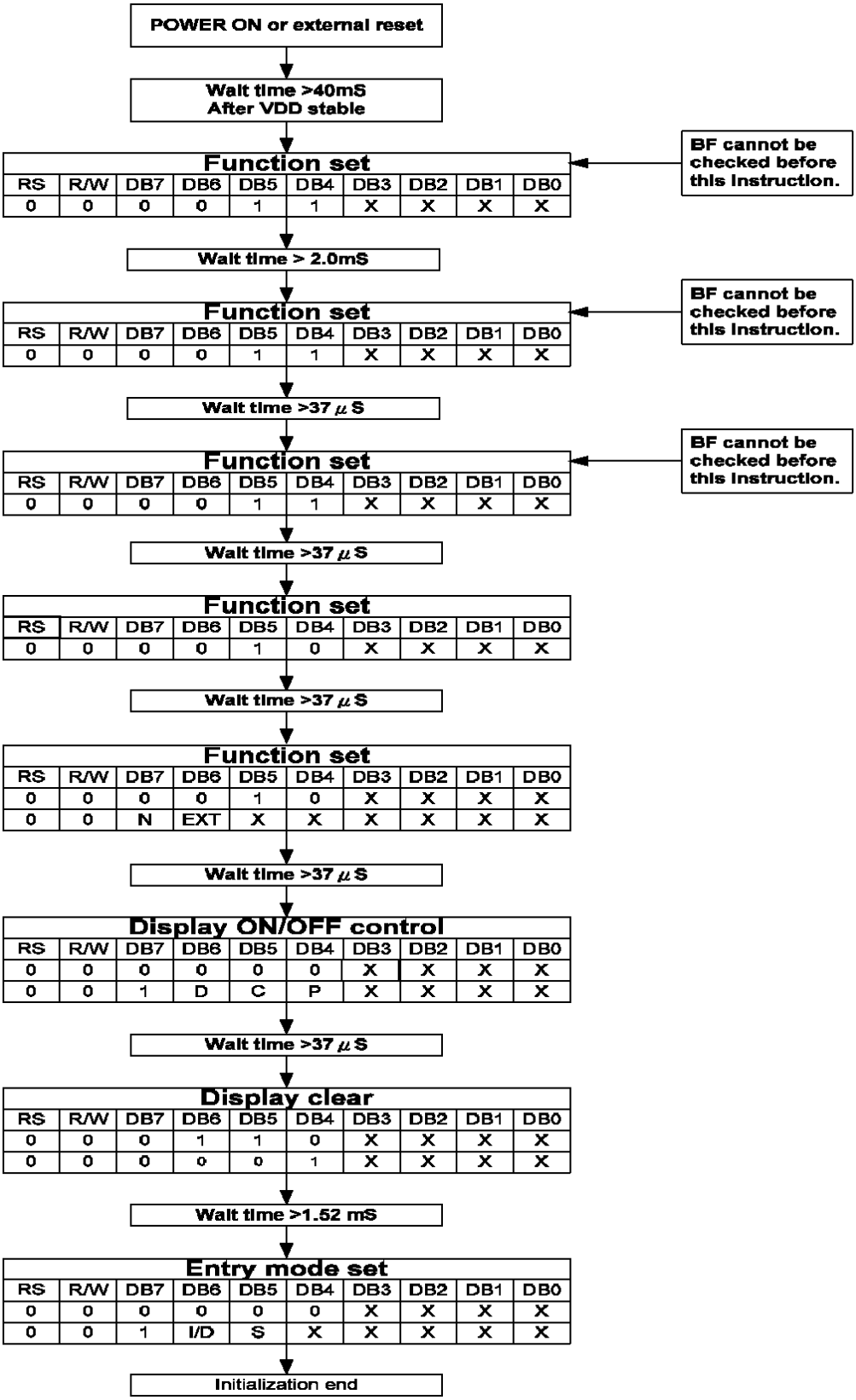
- t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
- Specified at 4.5V for 5V operation,and at 2.7V for 3V operation.
- For if 4.5V is not reached during 5V operation,teh internal reset circuit will not operate normally.

15.Initializing flow chart

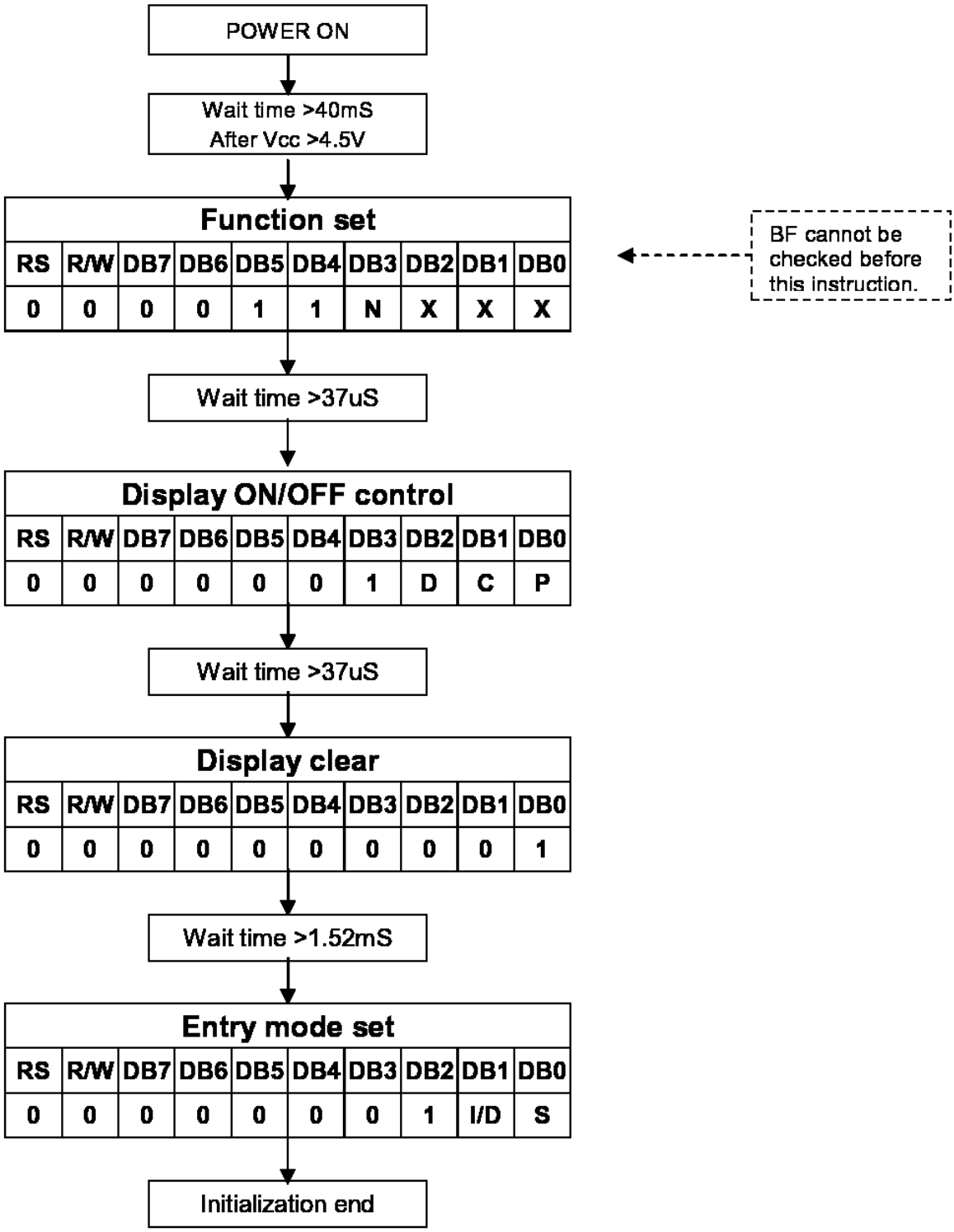
- **8-bit interface mode(fosc=270KHz)**


POWER ON
Wait time >40mS
After Vcc >4.5V
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 1 N X X X
BF cannot be checked before this instruction.
Wait time >37uS
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 1 N X X X
BF cannot be checked before this instruction.
Wait time >37uS
Display ON/OFF control
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 1 D C P
Wait time >37uS
Display clear
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 0 0 0 1
Wait time >1.52mS
Entry mode set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 0 1 I/D S
Initialization end

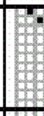
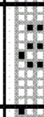
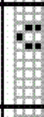
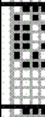
- **4-bit interface mode(fosc=270KHz)**


POWER ON or external reset
Wait time >40mS
After VDD stable
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 1 X X X X
BF cannot be checked before this instruction.
Wait time > 2.0mS
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 1 X X X X
BF cannot be checked before this instruction.
Wait time >37 μS
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 1 X X X X
BF cannot be checked before this instruction.
Wait time >37 μS
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 0 X X X X
Wait time >37 μS
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 0 X X X X
0 0 N EXT X X X X X X
Wait time >37 μS
Display ON/OFF control
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 1 D C P X X X X
Wait time >37 μS
Display clear
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 1 1 0 X X X X
0 0 0 0 0 1 X X X X
Wait time >1.52 mS
Entry mode set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 X X X X
0 0 1 I/D S X X X X X
Initialization end

- **Serial Interface (fosc=270KHz)**


POWER ON
Wait time >40mS
After Vcc >4.5V
Function set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 1 1 N X X X
BF cannot be checked before this instruction.
Wait time >37uS
Display ON/OFF control
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 1 D C P
Wait time >37uS
Display clear
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 0 0 0 1
Wait time >1.52mS
Entry mode set
RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
0 0 0 0 0 0 0 1 I/D S
Initialization end

16. Standard Character pattern

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)																
0001	(2)																
0010	(3)																
0011	(4)																
0100	(5)																
0101	(6)																
0110	(7)																
0111	(8)																
1000	(1)																
1001	(2)																
1010	(3)																
1011	(4)																
1100	(5)																
1101	(6)																
1110	(7)																
1111	(8)																

17. Revision records

Version	Ref.pages	Reversion Items	Date
A00	All Pages	New release	2010.08.25